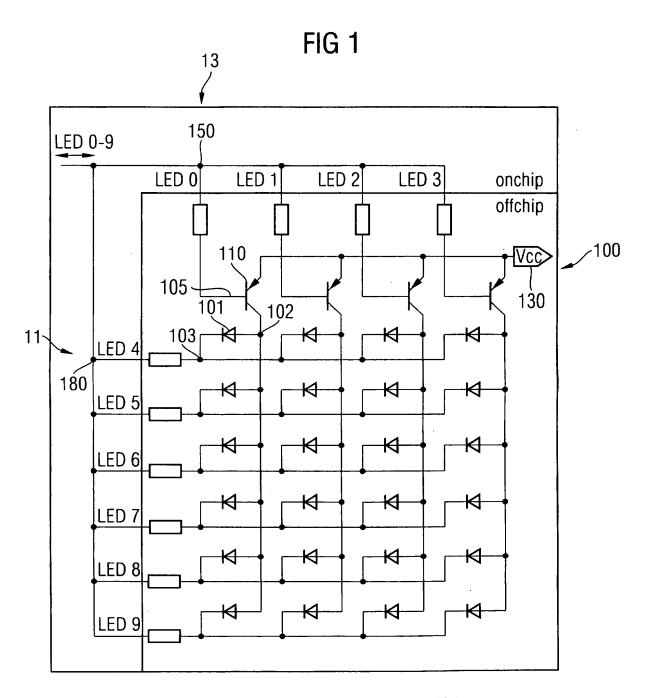


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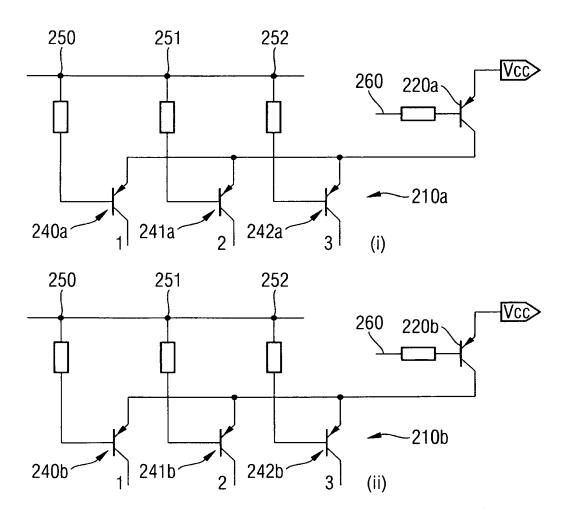


LED matrix as implemented in INCA-IP



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FIG 2



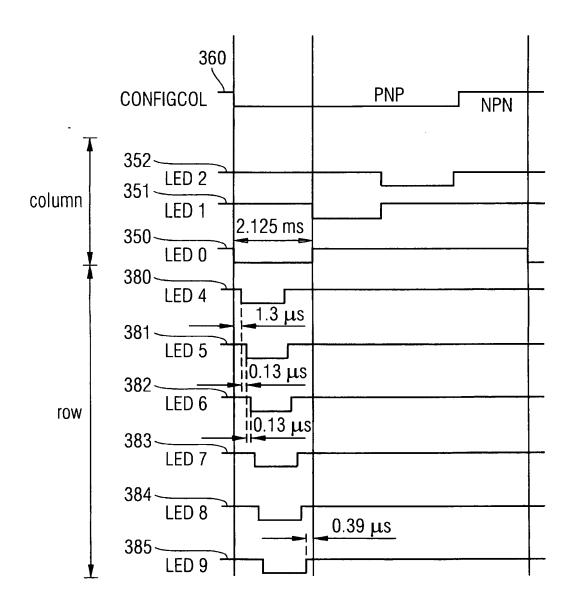
Row Decoding for output lines 1-4



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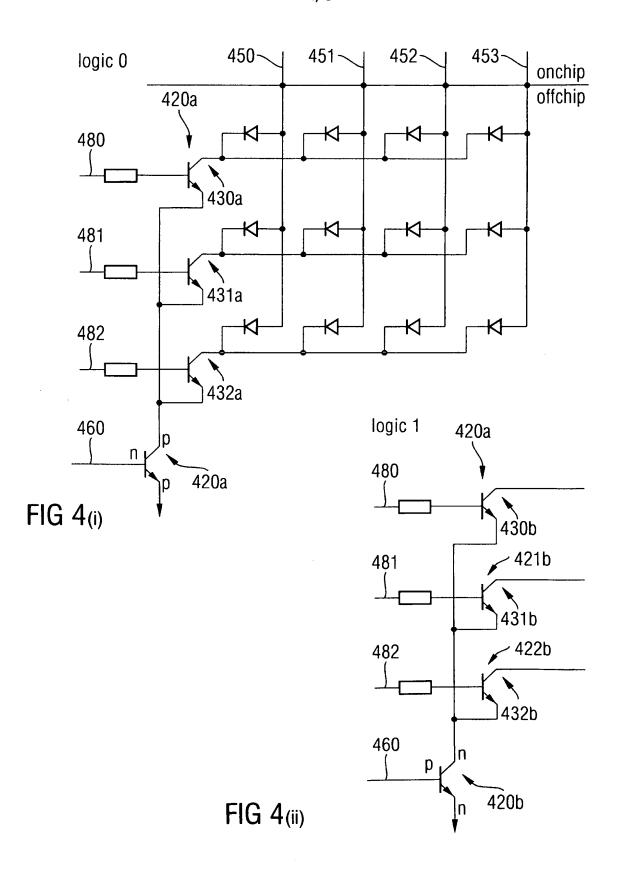
FIG 3



Timing Diagram of signals on LED output lines



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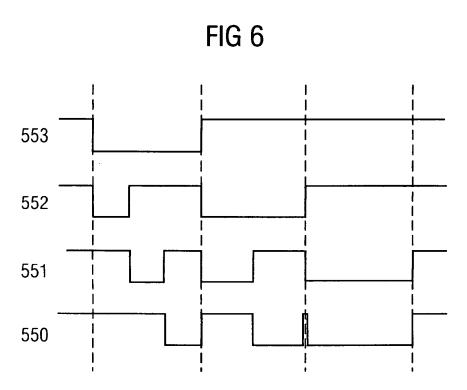
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5/6 Full-Decoding Vcc> (Prior Art) 520a Vcc> 551 552 550| 553 501 (i) 3 540a 541a 542a 520b Vcc> 550| 551 552 (ii) 502 540b 541b 520c Vcc> 550 551 (iii) 503 540c

Decoding technique using all the column control input

FIG 5





Timing Diagram with full-decoding